REMARKS/ARGUMENTS

This Amendment is submitted in response to the Office action of July 18, 2003. Claims 1, 4, 5 and 6 have been amended. Claims 1-7 are pending in the application. Applicant thanks the Examiner for attending to this application.

On page 2 of the action, claims 1-7 are rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,337,582 B1 issued to Yoshioka. Applicant respectfully traverses this rejection.

Claim 1 is rejected over Yoshioka. In the rejection, the Office action indicates that Yoshioka includes a static low swing driver stage (6, 8, 10). Regarding circuit 6, Yoshioka, in col. 10, lines 54-58, states "the source of the p-channel MOSFET 41a is connected to the power supply line of V_{cc} by way of the p-channel MOSFET 40a and at the same time, the source of the n-channel MOSFET 42a is connected to the ground by way of the n-channel MOSFET 43a." Similarly, regarding circuit 8, Yoshioka, in col. 9, lines 50-55, states "the source of the p-channel MOSFET 41b is connected to the power supply line of V_{cc} by way of the p-channel MOSFET 40b and at the same time, the source of the n-channel MOSFET 42b is connected to the ground by way of the n-channel MOSFET 43b." Also, for circuit 10, Yoshioka, in col. 10, lines 15-17, states, "[t]he source of the p-channel MOSFET 26b is connected to the power supply line of V_{cc} while the source of the n-channel MOSFET is connected to the ground."

Independent claim 1, as amended, recites a complementary pass transistor logic, a static driver connected to the complementary pass transistor logic, the static driver including a PMOS transistor and an NMOS transistor provided between at

least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal, and a charge recycling circuit. When a PMOS transistor and an NMOS transistor are provided between a power supply and an output terminal, the voltage swing level may change from ground level to V_{dd}-V_{th}. See, e.g., specification as filed, p. 14, lines 25-29, and FIG. 7. Similarly, when a PMOS transistor and an NMOS transistor are provided between the ground and the output terminal, the voltage swing level may change from V_{th} to V_{dd}. See, e.g., specification as filed, p. 14, lines 29-32, and FIG. 8. When a PMOS transistor and an NMOS transistor are provided between a power supply and an output terminal and between a ground and the output terminal, the voltage swing level may change from V_{th} to V_{dd}-V_{th}. See, e.g., specification as filed, p. 14, lines 32-35, and FIG. 9. Accordingly, claim 1 appears to be allowable over Yoshioka. In addition, claims 2 and 3 depending on claim 1, also therefore appear allowable over Yoshioka.

Claim 4 is rejected over Yoshioka. In the rejection, the Office action indicates that Yoshioka includes a static low swing driver stage (6, 8, 10). Regarding circuit 6, Yoshioka, in col. 10, lines 54-58, states "the source of the p-channel MOSFET 41a is connected to the power supply line of V_{cc} by way of the p-channel MOSFET 40a and at the same time, the source of the n-channel MOSFET 42a is connected to the ground by way of the n-channel MOSFET 43a." Similarly, regarding circuit 8, Yoshioka, in col. 9, lines 50-55, states "the source of the p-channel MOSFET 41b is connected to the power supply line of V_{cc} by way of the p-channel MOSFET 40b and at the same time, the source of the n-channel MOSFET 42b is connected to the ground by way of the n-

channel MOSFET 43b." Also, for circuit 10, Yoshioka, in col. 10, lines 15-17, states, "[t]he source of the p-channel MOSFET 26b is connected to the power supply line of V_{cc} while the source of the n-channel MOSFET is connected to the ground."

Independent claim 4, as amended, recites a complementary pass gate stage, a static low swing driver stage having a signal input to receive an input signal, the static driver stage including a PMOS transistor and an NMOS transistor provided between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal, and an equalization stage. When a PMOS transistor and an NMOS transistor are provided between a power supply and an output terminal, the voltage swing level may change from ground level to V_{dd}-V_{th}. See, e.g., specification as filed, p. 14, lines 25-29, and FIG. 7. Similarly, when a PMOS transistor and an NMOS transistor are provided between a ground and the output terminal, the voltage swing level may change from V_{th} to V_{dd}. See, e.g., specification as filed, p. 14, lines 29-32, and FIG. 8. When a PMOS transistor and an NMOS transistor are provided between a power supply and an output terminal and between a ground and the output terminal, the voltage swing level may change from V_{th} to V_{dd}-V_{th}. See, e.g., specification as filed, p. 14, lines 32-35, and FIG. 9. Accordingly, claim 4 appears to be allowable over Yoshioka.

Claim 5 is rejected over Yoshioka. In the rejection, the Office action indicates that Yoshioka includes a static low swing driver stage (6, 8, 10). Regarding circuit 6, Yoshioka, in col. 10, lines 54-58, states "the source of the p-channel MOSFET 41a is connected to the power supply line of V_{cc} by way of

the p-channel MOSFET 40a and at the same time, the source of the n-channel MOSFET 42a is connected to the ground by way of the n-channel MOSFET 43a." Similarly, regarding circuit 8, Yoshioka, in col. 9, lines 50-55, states "the source of the p-channel MOSFET 41b is connected to the power supply line of V_{cc} by way of the p-channel MOSFET 40b and at the same time, the source of the n-channel MOSFET 42b is connected to the ground by way of the n-channel MOSFET 43b." Also, for circuit 10, Yoshioka, in col. 10, lines 15-17, states, "[t]he source of the p-channel MOSFET 26b is connected to the power supply line of V_{cc} while the source of the n-channel MOSFET is connected to the ground."

Independent claim 5, as amended, recites a carry propagating circuit, a static low swing driver circuit receiving generate signals, the static driver circuit including a PMOS transistor and an NMOS transistor provided between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal, a pass gate network, an equalization circuit, and a latch circuit. When a PMOS transistor and an NMOS transistor are provided between a power supply and an output terminal, the voltage swing level may change from ground level to V_{dd}-V_{th}. See, e.g., specification as filed, p. 14, lines 25-29, and FIG. 7. Similarly, when a PMOS transistor and an NMOS transistor are provided between a ground and the output terminal, the voltage swing level may change from V_{th} to V_{dd}. See, e.g., specification as filed, p. 14, lines 29-32, and FIG. 8. When a PMOS transistor and an NMOS transistor are provided between a power supply and an output terminal and between a ground and the output terminal, the voltage swing level may

change from V_{th} to V_{dd}-V_{th}. See, e.g., specification as filed, p. 14, lines 32-35, and FIG. 9. Accordingly, claim 5 appears to be allowable over Yoshioka.

Claim 6 is rejected over Yoshioka. In the rejection, the Office action indicates that Yoshioka includes a static low swing driver stage (6, 8, 10). Regarding circuit 6, Yoshioka, in col. 10, lines 54-58, states "the source of the p-channel MOSFET 41a is connected to the power supply line of V_{cc} by way of the p-channel MOSFET 40a and at the same time, the source of the n-channel MOSFET 42a is connected to the ground by way of the n-channel MOSFET 43a." Similarly, regarding circuit 8, Yoshioka, in col. 9, lines 50-55, states "the source of the p-channel MOSFET 41b is connected to the power supply line of V_{cc} by way of the p-channel MOSFET 40b and at the same time, the source of the n-channel MOSFET 42b is connected to the ground by way of the n-channel MOSFET 43b." Also, for circuit 10, Yoshioka, in col. 10, lines 15-17, states, "[t]he source of the p-channel MOSFET 26b is connected to the power supply line of V_{cc} while the source of the n-channel MOSFET is connected to the ground."

Independent claim 6, as amended, recites a carry propagating circuit, a static low swing driver circuit receiving generate signals, the static driver circuit including a PMOS transistor and an NMOS transistor provided between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal, a pass gate network, an equalization circuit, and a latch circuit. When a PMOS transistor and an NMOS transistor are provided between the power supply and the output terminal, the voltage swing level may change from ground level to V_{dd}-V_{th}. See, e.g., specification as filed, p. 14, lines

25-29, and FIG. 7. Similarly, when a PMOS transistor and an NMOS transistor are provided between the ground and the output terminal, the voltage swing level may change from V_{th} to V_{dd}. See, e.g., specification as filed, p. 14, lines 29-32, and FIG. 8. When a PMOS transistor and an NMOS transistor are provided between a power supply and an output terminal and between a ground and the output terminal, the voltage swing level may change from V_{th} to V_{dd}-V_{th}. See, e.g., specification as filed, p. 14, lines 32-35, and FIG. 9. Accordingly, claim 6 appears to be allowable over Yoshioka. In addition, claim 7, depending on claim 6, also therefore appears allowable over Yoshioka.

In view of the foregoing remarks, it is respectfully submitted that this application is now in condition for allowance. Accordingly, reconsideration of the application and allowance of claims 1-7 are respectfully requested.

Respectfully submitted,
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